REMARKS

The Abstract of the Disclosure has been amended to reduce its length. In addition, the specification has been amended to correct a typographical error on page 4.

Claims 1-14 were in this patent application. Certain of these claims have been amended to even more succinctly clarify the invention, and claims 15-20 have been newly added. Claims 1-20 are now pending in this patent application.

Claims 1-3, 5-11, 13 and 14 were rejected under 35 U.S.C. 102(e) as being anticipated by Earnest (US 6,226,338), and claims 4 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in view of Begur et al. (US 5,784,649). These rejections are respectfully disagreed with, and are traversed below.

It is first pointed out that at least one patentably distinguishable feature of this invention can be seen by simply comparing Figure 2 of this patent application to Figures 2, 3 and 7 of Earnest. That is, in Figure 2 of this patent application it can be seen that there is a single dual port memory (RAM) 18, whereas in Earnest there is a transmit FIFO 16, a receive FIFO 18, and a corresponding transmit dual port RAM 100 and receive dual port RAM 200.

In order to further highlight this important distinction between this invention and Earnest claim 1 has been amended to recite in part that the programmable buffer circuit includes:

> "a single dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;
>
> an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for selectively storing data in and reading data from said single dual port memory;
>
> an address generator for generating dual port memory addresses for selectively

> reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus; and
>
> an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory." (emphasis added)

In addition, the independent method claim 9 has been amended to also recite the use of a single dual port memory, and to state that generating dual port memory addresses is for "selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus."

Claims 1 and 9, as even further clarified by amendment, are clearly not anticipated or rendered unpatentable by the two FIFO, two dual port RAM embodiment disclosed by Earnest. For example, Earnest states in col. 2, line 66, to col. 3, line 6:

> "Core 14 is coupled to DMA controller 20 through transmit FIFO 16 and receive FIFO 18. Transmit FIFO 16 and receive FIFO 18 each include a single random access memory (RAM) device for buffering data between core 14 and DMA controller 20. The memory locations within each RAM device are divided into blocks, or "queues", with one queue being associated with a corresponding one of the logical channels."

Reference can also be made to col. 4, lines 33-36:

> "The data communication circuit shown in FIG. 1 uses a single memory device for all logical channels in transmit FIFO 16 and a single memory device for all logical channels in receive FIFO 18."

Clearly there is no express disclosure of, or a suggestion to, provide a programmable buffer circuit and method that includes a single dual ported memory device.

In that claims 1 and 9 are not anticipated by Earnest, then claims 2-8 and 10-14 are not anticipated by Earnest, nor or they rendered unpatentable over Earnest alone or in view of Begur et al.

Note, for example, that claims 2 and 10 both refer to a programmable ability to provide operation of channel buffers in a block access mode or in a FIFO access mode. It is clear that Earnest discloses operation only in the FIFO mode. Both of these claims have been further clarified to recite, as in claim 2, that the control unit is programmable for operating individual ones of channel buffers in "one of a block access mode and in a first in/first out (FIFO) access mode of operation".

Claims 1-14 are thus believed to be clearly patentable over Earnest, either alone or in combination with Begur et al., and the Examiner is respectfully requested to reconsider and remove the rejections in view of the claims as now presented for examination.

Claims 15-20 are newly added, and are also deemed to be patentable over the prior art that was cited and relied on by the Examiner. For example, claim 15 states that a programmable buffer circuit has a control unit programmable by a data processor for specifying:

> "for individual ones of buffers both buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, where said control unit is programmable for operating individual ones of said buffers in one of a block access mode of operation and in a first in/first out (FIFO) access mode of operation."

Claims 15 and 16 are clearly patentable over Earnest, either alone or in combination with Begur et al.

Claim 17 recites in part that a programmable buffer circuit has a control unit programmable by a data processor for specifying:

> "a control unit programmable by said data processor for specifying individual ones of buffer locations and buffer sizes within said dual port memory for individual ones of said channel interfaces, where there are four transmit registers

> allocated for each channel interface designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1 and four receive registers also designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1, said control unit being responsive to operating in a Block Mode to provide two independent buffers Buffer0 and Buffer1, where BaseReg0 stores the starting address of Buffer0, SizeReg0 specifies the size of Buffer0, BaseReg1 stores the starting address of Buffer1, and SizeReg1 specifies the size of Buffer1 size, said control unit being further responsive to operating in a FIFO Mode to provide one buffer, where BaseReg0 stores the start address of the single buffer, and SizeReg0 specifies the size of the single buffer."

Dependent claim 18 further specifies the operation in the FIFO Mode where the "register BaseReg1 functions as a Low Threshold Register and said register SizeReg1 functions as a High Threshold Register."

Support for claims 17 and 18 is found at least at page 6, line 21, to page 7, line 4, and no new matter is added.

Claims 17 and 18 are clearly patentable over Earnest, either alone or in combination with Begur et al.

Claim 19 recites in part that a programmable buffer circuit has a control unit programmable by a data processor, where the control unit is operable to:

> "set up and operate a first portion of said dual port memory in a block mode of operation having a transmit buffer and a receive buffer, and to also operate a second portion of the dual port memory in a FIFO mode of operation having a single buffer."

Dependent claim 20 then further modifies claim 19 by stating that the "first portion of said dual port memory is coupled to a data packet channel interface, and where said second portion of said dual port memory is coupled to an audio CODEC".

Support for claims 19 and 20 is found at least at page 11, lines 11-25, and no new matter is

added.

Claims 19 and 20 are also clearly patentable over Earnest, either alone or in combination with Begur et al.

A favorable reconsideration that results in the allowance of all of the pending claims is respectfully requested.

Respectfully submitted:

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